PATENT ABSTRACTS OF JAPAN

(11)Publication number : **10-161080**
(43)Date of publication of application : **19.06.1998**

(51)Int.CI. G02F 1/133
G02F 1/133

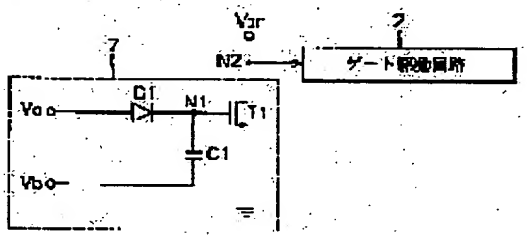
(21)Application number : **09-255479**
(22)Date of filing : **19.09.1997**

(71)Applicant : **SAMSUNG ELECTRON CO LTD**
(72)Inventor : **KEN ZENNEI**
BUN SHOKAN
RI CHUMAN
RI KEIKON

(30)Priority
Priority number : **96 9658389** Priority date : **27.11.1996** Priority country : **KR**

(54) POWER-OFF DISCHARGE CIRCUIT FOR LIQUID CRYSTAL DISPLAY DEVICE AND LIQUID CRYSTAL DISPLAY DEVICE USING THE SAME

(57)Abstract:
PROBLEM TO BE SOLVED: To provide the power-off discharge circuit of a liquid crystal display device capable of charging the voltage of a gate line on which a gate-on voltage is impressed at the time of a power-on quickly.
SOLUTION: This circuit includes a transistor T1 which has a gate, a source and a drain and in which the drain is connected to the gate-on terminal of a gate on/off voltage generator 2 and the source is grounded and which is turned on or turned off according to a gate voltage, a diode D1 to the anode of which a first voltage is applied and whose cathode is connected to the gate of the transistor T1 and a capacitor C1 to one terminal of which a second voltage is applied and whose other terminal is connected to the contact N1 between the cathode of the diode D1 and the gate of the transistor T1. The transistor T1 is turned on by the potential of the contact N1 in a power-on state and the transistor T1 is turned off by the potential of the contact N1 at the time of power-off state.



LEGAL STATUS

[Date of request for examination] 08.06.1999

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]	3150929
[Date of registration]	19.01.2001
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the electric discharge circuit for LCDs (LCD:Liquid Crystal Display), and in detail, when a LCD carries out a power off, it relates to the circuit for making the gate ON state voltage charged by the liquid crystal panel discharge.
[0002]
[Description of the Prior Art] The liquid crystal capacitor and hold capacitor (storage capacitor) with which one pixel was connected with one TFT and the aforementioned TFT in the general TFT LCD It is constituted. The aforementioned TFT acts on the aforementioned liquid crystal capacitor as a switch for impressing a voltage. In the turn-on status of the aforementioned transistor, the aforementioned liquid crystal capacitor is charged with a gradation voltage. It prevents that the aforementioned hold capacitor is connected with the liquid crystal capacitor and the parallel, and the voltage charged by the liquid crystal capacitor in the turn-off status of the aforementioned transistor is revealed. Let a voltage required here to carry out the turn on of the aforementioned TFT into gate ON state voltage, and let a voltage required to carry out a turn-off be gate OFF state voltage. In an application, the aforementioned gate ON state voltage is actually more than 20V, and gate OFF state voltage is less than [-7V]. It is asked for the gate-on / OFF state voltage in which a liquid crystal panel has larger large-sized-izing and such DC [that it is made highly minute] level. The light transmittance of liquid crystal is controlled in the pixel to which the voltage charged by the liquid crystal capacitor in such a TFT LCD corresponds, and a color specification is made by this.
[0003] Hereafter, the TFT LCD which has the panel structure of the general preceding paragraph gate with reference to an accompanying drawying is explained. it is shown in drawing 1 -- as -- the above -- a general TFT LCD consists of the timing-control circuit 1, the gate drive circuit 2, the source drive circuit 3, a gradation voltage generator 4, a liquid crystal panel 5, and gate-on / OFF-state-voltage generator 6
[0004] The aforementioned timing-control circuit 1 is a chrominance signal (RGB), a synchronizing signal (Hsync, Vsync), and a clock signal (CLK). It is connected so that it may be inputted, and the gate drive circuit 2 and the source drive circuit 3 are provided with the output of the aforementioned timing-control circuit 1. The output of the gradation voltage generator 4 is the gate-on / OFF state voltage (Von, Voff) which is connected so that it may be provided for the source drive circuit 3, and is outputted from gate-on / OFF-state-voltage generator 6. It is connected so that it may be provided for the gate drive circuit 2. A liquid crystal panel 5 consists of the data lines D1-Dm of the masses which intersect a perpendicular at many gate lines G0-Gn and this, respectively. The gate drive circuit 2 is connected with each aforementioned gate line, and the source drive circuit 3 is connected with each aforementioned data line. If a liquid crystal panel 5 is guessed in detail, one TFT, one hold capacitor Cst, and one liquid crystal capacitor Cp exist in the field to which each gate line and a data line cross. The gate of the aforementioned TFT is connected with a gate line, the source is connected with a corresponding data line and the liquid crystal capacitor Cp and the hold capacitor Cst are connected with a drain in parallel. Other terminals of a liquid crystal capacitor are connected with a common electrode, and other terminals

of a hold capacitor are connected with the gate line of the preceding paragraph. Therefore, the ends voltage of a liquid crystal capacitor is determined by the data-line voltage which corresponds with common electrode voltage, and the ends voltage of a hold capacitor is determined by a corresponding data-line voltage and the corresponding gate line voltage of the preceding paragraph. In the liquid crystal panel which has preceding paragraph gate structure especially, the pixel is not most connected with the gate line G0 of scale division. Since preceding paragraph gate link structure has the advantage in which a numerical aperture becomes high compared with the independent wiring method with which a hold capacitor is connected by the special line, it is applied widely.

[0005] The timing-control circuit 1 is chrominance-signal RGB, synchronizing signal Hsync, and Vsync. And the timing of a chrominance signal is controlled using a clock signal CLK, and the control signal for operating the drive circuits 2 and 3 is generated. The gradation voltage generator 4, and the gate-on / OFF-state-voltage generator 6 generate many gradation voltages, and gate-on / OFF state voltage, respectively. The source drive circuit 3 is provided with the gradation voltage of the aforementioned masses, and the gate drive circuit 2 is provided with gate-on / OFF state voltage. Using the signal outputted from gate-on / OFF state voltage, and the timing-control circuit 1, each gate line generates the gate driver voltage of 1 horizontal-scanning time to which a between turn on is made to be carried out one by one, and the gate drive circuit 2 impresses the gate driver voltage by which generation was carried out [aforementioned] to each gate line. Here, 1 horizontal-scanning time is time consumed by impressing a data driver voltage to all the pixels connected with one gate line. The source drive circuit 3 impresses the voltage which chose and chose one of gradation voltages according to the chrominance signal outputted from the timing-control circuit 1 to each data line to a corresponding data line. Subsequently, each aforementioned data-line voltage is recorded on the pixel of one line connected with the gate line which is in the turn-on status.

[0006] Drawing 2 shows an example of the gate driver voltage applied to the TFT LCD which has the aforementioned preceding paragraph gate panel structure. When drawing 2 is referred to, arbitrary 1 gate lines (Gn-1) understand that the between turn on of the 1 horizontal-scanning time is carried out among one frame, and a turn-off is carried out in the remaining section. Moreover, the turn on of each gate line is carried out one by one.

[0007] When it is gate-on / OFF state, the operation in a liquid crystal panel is explained in detail. For example, when gate ON state voltage is impressed to the gate line G1 in drawing 1 and gate OFF state voltage is impressed to the remaining gate line, the turn on of all the TFT of one line connected with the gate line G1 is carried out. Subsequently, the data driver voltage offered through a data line (D1-Dm) from the source drive circuit 3 is impressed to the liquid crystal capacitor Cp1 and the hold capacitor Cst1 via the TFT by which the turn on was carried out [aforementioned]. The liquid crystal capacitor Cp1 is charged by this with the voltage applicable to the differentiation between a data driver voltage and common electrode voltage, and the hold capacitor Cst1 is charged with the voltage applicable to the differentiation between a data driver voltage and the gate OFF state voltage of the preceding paragraph gate line G0. Moreover, the hold capacitor Cst2 of the following line connected with the aforementioned gate line G1 by the gate ON state voltage currently impressed to the gate line G1 is charged. Since the ends voltage of the aforementioned hold capacitor Cst2 is larger than the voltage of the liquid crystal capacitor Cp2 in the gate off section, the liquid crystal capacitor Cp2 continues a charge by this and it is supplied, the liquid crystal capacitor Cp2 can make the voltage impressed at the time of gate-on hold.

[0008] When a user makes a power switch turn off in this status or an external power is intercepted by the grounds, such as electric power failure, some time requires the charge charged by the hold capacitor and liquid crystal capacitor in a liquid crystal panel for discharging completely. Since the turn-off of the TFT is carried out and a drain terminal will be in the floating (floating) status if power is intercepted, this is for the charge charge of a hold capacitor and a liquid crystal capacitor to discharge automatically. By this, even if a user intercepts current supply, there is a trouble where a screen disappears gradually by slow charge electric discharge.

Moreover, the problem that liquid crystal deteriorates is in a liquid crystal capacitor immediately after the aforementioned power cutoff by [of the time are predetermined in direct current voltage] carrying out the object for intercroppings.
[0009] In order to solve the above troubles, a South Korean patent-application [of No. 29444 / 95 to]" TFT LCD ******s by these people, and it applies for a circuit and its drive technique." Shortly after the aforementioned "TFT LCD ******s and a power off is carried out in a circuit and its drive technique", the voltage of the gate off terminal of gate-on / OFF-state-voltage generator is made to discharge quickly. In the power-on status, the aforementioned gate off terminal is substantially connected with the gate line in a liquid crystal panel by switching of a gate drive circuit. For example, when 400 gate lines exist, gate OFF state voltage is impressed to 399 gate lines, and gate ON state voltage is impressed to one gate line. By making the voltage of a gate off terminal discharge immediately after a power off, the above-mentioned patent is removing quickly the charge charged by the hold capacitor and liquid crystal capacitor of a panel.
[0010]
[Problem(s) to be Solved by the Invention] However, in the above-mentioned conventional patent, the charge charge by the liquid crystal capacitor and hold capacitor which are connected with the gate line by which gate OFF state voltage was impressed just before the power off is removed. Therefore, there is a trouble a screen not only still disappears late, but where the degradation by direct-current stress occurs in the pixel by which gate ON state voltage was impressed just before the power off.
[0011] Therefore, this invention is for solving the aforementioned conventional trouble, and the purpose is in offering the power-off electric discharge circuit of the LCD which can make the voltage of the gate line to which gate ON state voltage was impressed at the time of a power off discharge quickly.
[0012]
[Means for Solving the Problem] The power-off electric discharge circuit according to this invention is applied to the LCD containing the liquid crystal panel which has preceding paragraph gate link structure. The aforementioned liquid crystal panel consists of a data line of the masses which intersect many gate lines and this, and the pixel is formed in the field to which each aforementioned gate line and a data line cross. The aforementioned pixel consists of TFT, a liquid crystal capacitor, and a hold capacitor. The gate of TFT is connected with a corresponding gate line, the source is connected with a corresponding data line and any 1 terminal of a liquid crystal capacitor and a hold capacitor is connected common to the drain of the aforementioned TFT. Other terminals of a liquid crystal capacitor are connected with a common electrode, and other terminals of a hold capacitor are connected with the gate line of the preceding paragraph.
[0013] Such a LCD contains the gate drive circuit connected with each gate line of the aforementioned liquid crystal panel at the same time it is connected with gate-on of the gate-on / OFF-state-voltage generator, and the aforementioned voltage generator which have gate-on and a gate off terminal, and a gate off terminal. The aforementioned gate-on / OFF-state-voltage generator generate gate ON state voltage and gate OFF state voltage, and provides the aforementioned terminal with them, and it is impressed by the gate line which corresponds the voltage chosen and chosen in one of the aforementioned gate-on or OFF state voltage to each gate line according to a control signal predetermined in the aforementioned gate drive circuit. At this time, a control signal is beforehand determined that the turn on of each gate line is carried out one by one.
[0014] In order to attain the aforementioned purpose, a drain is connected with the gate-on terminal of the aforementioned gate-on / OFF-state-voltage generator, and the power-off electric discharge circuit according to this invention contains the power-off sensing circuit which provides with bias voltage the gate of a transistor and the aforementioned transistor where the source is grounded. The aforementioned power-off sensing circuit generates the bias voltage for carrying out the turn-off of the aforementioned transistor in the power-on status, and generates the bias voltage for carrying out the turn on of the aforementioned transistor in the power-off status. Therefore, when the turn on of the aforementioned transistor is carried out by the aforementioned

power-off sensing circuit in the power-off status, the voltage of a gate-on terminal discharges quickly through the current path formed of the aforementioned transistor and a grounding.
[0015] When the characteristic feature of this invention is followed, the diode and the end by which the 1st voltage was connected with the anode are connected with the cathode of the aforementioned diode, and the aforementioned power-off sensing circuit consists of a capacitor with which the other end is connected with the 2nd voltage. The contact of the aforementioned diode and a capacitor is connected with the gate of the aforementioned transistor. the time of the threshold voltage of Vth1 and the aforementioned transistor being called Vth2 for the threshold voltage of the aforementioned diode -- the 1st aforementioned voltage -- (Vth1+Vth2) -- the parvus -- things -- desirable -- the 2nd aforementioned voltage -- [the 1st voltage - (Vth1+Vth2)] -- the parvus -- things are desirable Moreover, as the 1st aforementioned voltage, a grounding or a negative voltage is desirable. In such conditions, when it is in the power-on status, the potential of the contact of the aforementioned diode and a capacitor is the voltage which descended about one threshold voltage Vth of the aforementioned diode in the 1st voltage. Therefore, when the aforementioned transistor is NMOS (N-type Metal Oxide Semiconductor), the turn-off of the aforementioned transistor is carried out by the potential of the aforementioned contact. Moreover, the aforementioned capacitor is charged with the voltage applicable to the potential of the aforementioned contact, and the differentiation between the 2nd voltage. if power is intercepted at this time -- the [the aforementioned 1st voltage value and] -- 2 voltage value becomes a zero. Since a capacitor has the attribute which is going to hold an ends voltage, the potential of the aforementioned contact becomes a value larger than the minimum threshold voltage Vth2. By this, the turn on of the aforementioned transistor is carried out by the potential of the aforementioned contact larger than threshold voltage Vth2, and the voltage of a gate-on terminal may discharge quickly.
[0016] When other characteristic features of this invention are followed, the aforementioned power-off sensing circuit consists of a capacitor connected between the voltage terminal of the positive of the resistance connected between the input terminals of an inverter and the aforementioned inverter and the voltage terminals of a positive equipped with the input terminal, the output terminal, the voltage terminal of a positive, and the earth terminal, and the aforementioned inverter, and the earth terminal. Supply voltage is impressed to the input terminal of the aforementioned inverter, and the output terminal of the aforementioned inverter is connected with the gate of the aforementioned transistor. The aforementioned inverter provides an output terminal with the voltage of the voltage terminal of a positive, when supply voltage is a low, and when supply voltage is high-level, it provides an output terminal with grounding level. In the power-on status, the aforementioned supply voltage is high-level, and the aforementioned supply voltage is a low in the power-off status. Therefore, in the power-on status, the voltage of the output terminal of the aforementioned inverter is set to grounding level, and turns into the voltage of the voltage terminal of a positive in the power-off status. In the power-on status, since the output of an inverter is grounding level, the turn-off of the aforementioned transistor is carried out continuously. The voltage of the voltage terminal of the aforementioned positive is the value for which the time constant as which the aforementioned supply voltage is determined by the aforementioned resistance and the capacitor was delayed. If it changes to the power-off status in the power-on status, supply voltage serves as a low, and after holding only the time on which it decides with the aforementioned time constant in the voltage terminal of the aforementioned positive at high-level supply voltage, it will fall in a low. While the aforementioned supply voltage falls in a low and is held high-level in the voltage terminal of the aforementioned positive, the aforementioned inverter outputs the voltage of the voltage terminal of the high-level aforementioned positive. By this, the voltage outputted from the aforementioned inverter can carry out the turn on of the aforementioned transistor, and gate ON state voltage can discharge through the aforementioned transistor.
[0017]
[Embodiments of the Invention] Hereafter, the desirable operation gestalt of this invention is explained in detail based on an accompanying drawying. Drawing 3 is a block diagram of the

LCD to which the power-off (Von) electric discharge circuit according to the 1st operation gestalt of this invention was applied, and as shown in this drawing, the LCD to which the power-off electric discharge circuit according to the 1st operation gestalt of this invention was applied consists of the timing-control circuit 1, the gate drive circuit 2, the source drive circuit 3, the gradation voltage generator 4, a liquid crystal panel 5, gate-on / OFF-state-voltage generator 6, and a gate ON-state-voltage electric discharge circuit 7.

[0018] The same sign is attached about the same thing as the component of a LCD shown in drawing 1 among the aforementioned components. As mentioned above, a liquid crystal panel 5 is preceding paragraph gate link structure, and the gate ON-state-voltage electric discharge circuit 7 according to the example 1 of this invention is connected with the gate-on terminal between gate-on / OFF-state-voltage generator 6, and the gate drive circuit 2.

[0019] Drawing 4 shows the gate ON-state-voltage electric discharge circuit 7 of drawing 3 in detail. Reference of drawing 4 constitutes the gate ON-state-voltage electric discharge circuit 7 from a transistor T1, diode D1, and a capacitor C1. The aforementioned transistor T1 is NMOS, a drain is connected with the aforementioned gate-on terminal and the source is grounded. The 1st voltage Va is impressed to the anode of diode D1, and a cathode is connected with the gate of the aforementioned transistor T1. The 2nd voltage Vb is impressed to the end of the aforementioned capacitor C1, and it connects with the contact N1 of the cathode of the aforementioned diode D1, and the gate of the aforementioned transistor T1 at the other end. The threshold voltage of Vth1 and the aforementioned transistor T1 is assumed to be Vth2 for the threshold voltage of the aforementioned diode D1.

[0020] Next, the operation of a gate ON-state-voltage electric discharge circuit which follows the 1st operation gestalt of this invention with reference to the drawing 4 and the drawing 5 is explained. When it is in the power-on status, you have to make potential of the aforementioned contact N1 smaller than the threshold voltage Vth2 of the aforementioned transistor T1. This is because the turn-off of the aforementioned transistor must be carried out so that the electric discharge in the gate-on terminal by the transistor T1 may not happen in the power-on status. Since the potential of the contact N1 in the power-on status is expressed by Va-Vth1, the formula of Va-Vth1<Vth2 is materialized. Therefore, the formula of Va<Vth1+Vth2 must fill.

[0021] Moreover, since the 2nd aforementioned voltage Vb serves as grounding level in the power-off status, the potential of the aforementioned contact N1 becomes the voltage charged to the ends of a capacitor C1 in the power-on status. Such an operation is usually called charge pumping. Since the turn on of the aforementioned transistor T1 must be carried out in the power-off status, in the power-on status, you have to make the ends voltage of the aforementioned capacitor larger than the threshold voltage Vth2 of the aforementioned transistor T1. It is as follows if this is expressed with a formula.

[0022] (Va-Vth1)-Vb> Vth2 and this formula are Vb<Va. - (Vth1+Vth2)
But it is expressed. The 1st voltage was assumed to be grounding level 0V, and the 2nd voltage was assumed [in / the 1st operation gestalt of this invention / in order to fulfill the above bias conditions] to be -10V. Here, threshold voltage Vth1 and Vth2 usually considers on a target that it is 0.7V.

[0023] In the power-on status, the turn on of the diode D1 is carried out, and a capacitor C1 holds the voltage applicable to the differentiation between the potential of a contact N1, and the 2nd voltage Vb. As shown in drawing 5 , the potential VN1 of a contact N1 is -0.7V. The aforementioned -0.7V carry out the turn-off of the transistor T1, and the gate drive circuit 2 is provided with the voltage Von of a gate-on terminal.

[0024] If it goes into the power-off status that an external power is intercepted in this status, the 2nd voltage Vb will be set to grounding level 0V, and the potential VN1 of a contact N1 will become the ends voltage of a capacitor C1 by the charge pumping. In the power-on status, since the ends voltage of the aforementioned capacitor C1 is the differentiation between the potential VN1 of a contact N1, and the 2nd voltage Vb, it is set to -0.7-(-10) =9.3V.

[0025] When drawing 5 is referred to, the immediately after [a power off] 2nd voltage Vb is set to grounding level 0V, and it turns out that the potential VN1 of a contact N1 is set to 9.3V. The

aforementioned 9.3V decrease gradually by natural electric discharge of a capacitor C1. Therefore, the turn on of the transistor T1 is carried out by the aforementioned 9.3V gate voltage, and the voltage Von of the gate-on terminal shown in drawing 5 discharges quickly.

[0026] The power-off sensing circuit using the charge pumping of the 1st and 2nd voltage beforehand assumed in the 1st operation gestalt of this invention mentioned above and a capacitor is indicated. The aforementioned power-off sensing circuit provides a transistor with the bias conditions searched for in this invention. By carrying out the turn on of the aforementioned transistor immediately after a power off, the voltage of a gate-on terminal can be discharged quickly.

[0027] Next, the gate ON-state-voltage electric discharge circuit 8 which follows the 2nd operation gestalt of this invention with reference to the drawing 6 and the drawing 7 is explained. The gate ON-state-voltage electric discharge circuit 8 according to the 2nd operation gestalt of this invention is connected with the gate-on terminal between gate-on / OFF-state-voltage generator 6 of drawing 3 , and the gate drive circuit 2 like the aforementioned 1st operation gestalt.

[0028] Reference of drawing 6 constitutes the gate ON-state-voltage electric discharge circuit 8 according to the 2nd operation gestalt of this invention from resistance R1, R2, and R3 of 4 or 3 NMOS transistors T3 and T of 2 or 2 PMOS (P-type Metal Oxide Semiconductor) transistor T, and two capacitors C2 and C3. The two aforementioned transistors T2 and T3 are CMOS (Complementary Metal Oxide Semiconductor). It consists of an inverter. As for the two aforementioned transistors T2 and T3, each drain and the gate are connected mutually. The common gate of the two aforementioned transistors T2 and T3 is an input edge, and a common drain is an outgoing end. Supply voltage Vcc is impressed to the aforementioned input edge, and this voltage Vcc is 5V usually used in the system. Resistance R1 is connected between the source of the aforementioned transistor T2, and an input edge, and the source of the aforementioned transistor T3 is grounded. A capacitor C2 is connected between the source of the aforementioned transistor T2, and a grounding. As for the drain of a transistor T4, resistance R3 is connected with the contact N2 between a gate-on terminal and the gate drive circuit 2 as a medium, and the source is grounded. A capacitor C3 is connected between the gate of the aforementioned transistor T4, and a grounding, and resistance R2 is connected between the common drain of the two aforementioned transistors T2 and T3, and the gate of the aforementioned transistor T4.

[0029] In the 2nd operation gestalt of this invention, the threshold voltage of -1.5V and the aforementioned transistors T3 and T4 was assumed to be 1.5V for the threshold voltage of the aforementioned transistor T2. In the 2nd operation gestalt of this invention, the power-off detection method for sensing the power-off status using supply voltage VCC, an inverter, and a resistance-capacitor circuit was applied.

[0030] In the power-on status that the external power is supplied normally, the aforementioned supply voltage VCC is 5V. The turn on of the transistor T3 of an inverter is carried out by 5V impressed to the input edge Vin, and the potential of outgoing end Vout is set to grounding level 0V. The potential of aforementioned 0V carries out the turn-off of the transistor T4, and the gate drive circuit 2 is provided with the voltage of a gate-on terminal without discharging.

[0031] If it rushes into the power-off status in this status, supply voltage VCC will fall in grounding level 0V. Since the resistance R1 and the capacitor C2 constitute an in-series RC circuit, supply voltage VCC appears, after [which is determined with resistance and capacitance in the contact of two elements R1 and C2] delaying by the time constant. Then, the voltage charged by the capacitor C2 discharges automatically. If drawing 7 is referred to, supply voltage VCC falls abruptly immediately after a power off grounding level 0V, and after the potential Vc of the contact of resistance R1 and the capacitor C2 holds between 5V of the time t1 on which it decides with the aforementioned time constant from a power-off time, it will fall gradually.

[0032] Between the aforementioned time t1, the gate-source voltage of a transistor T2 is -5V, and the turn on of the transistor T2 is carried out for the aforementioned gate-source voltage by the parvus's from threshold voltage. According to this, the common-drain voltage of two transistors T2 and T3 becomes the potential Vc of the aforementioned contact. The aforementioned

common-drain voltage makes a capacitor C3 charge, and the potential Vd of the contact of the aforementioned resistance R2 and the capacitor C3 rises to 4V. Here, going up to 4V is for the potential Vc of a contact to descend in part by resistance R2. The wave from which the potential Vd of the aforementioned contact changes according to time is shown in drawing 7 . The turn on of the aforementioned transistor T4 is carried out at the moment of exceeding 1.5V whose potential of the aforementioned contact Vd is the threshold voltage of a transistor T4 in the aforementioned time section t1. That is, in the section where the potential Vd of the aforementioned contact is higher than 1.5V, the turn on of the aforementioned transistor T4 is always carried out. The voltage of a gate-on terminal discharges quickly by the turn on of the aforementioned transistor T4, and the potential of a contact N2 falls quickly, as shown in drawing 7 .

[0033] Progress of the aforementioned time section t1 reduces the potential Vc of a contact gradually by electric discharge of a capacitor C2, as shown in drawing 7 . Also at this time, if the potential Vc of a contact is larger than 1.5V, the turn on of the transistor T2 will be carried out for a gate-source voltage by the parvus's from -1.5V. While the aforementioned transistor T2 is a turn on, the potential Vd of a contact changes almost like the potential Vc of a contact. Therefore, the potential Vd of a contact will also fall gradually from 4V, if the time section t1 passes.

[0034] If the potential Vc of the aforementioned contact becomes lower than 1.5V, the turn-off of the transistor T2 will be carried out, and the ends voltage of a capacitor C3 will discharge automatically. The section t2 where the potential Vc of the aforementioned contact is larger than 1.5V is determined by a capacitor C3 and the time constant of resistance R2. That is, decision of the time when it is required for making the voltage of a gate-on terminal discharge completely must carry out the turn on of the transistor between things T4 longer than this time. And the time constant determined by the aforementioned resistance R2 and the capacitor C3 can adjust the turn-on time of the aforementioned transistor T4.

[0035] The gate ON-state-voltage electric discharge circuit according to the aforementioned 2nd operation gestalt carries out the turn on of the transistor T4 only in the power-off status, and is made to discharge the voltage of a gate-on terminal. On the other hand, in the aforementioned 2nd operation gestalt, the common-drain terminal of two transistors T2 and T3 can be directly connected with the gate of a transistor T4. In this case, the time constant determined by resistance R1 and the capacitor C2 can adjust the turn-on time of a transistor T4.

[0036]

[Effect of the Invention] As mentioned above, the power-off electric discharge circuit according to this invention senses the power-off status, and the voltage of a gate-on terminal is made to discharge immediately after a power off quickly. Therefore, the LCD to which this invention is applied can prevent that the picture image by the pixel line on the panel by which gate ON state voltage was finally impressed after the power off disappears gradually. Moreover, the power-off electric discharge circuit according to this invention can prevent a degradation of the liquid crystal by direct-current stress by making the gate ON state voltage which remains on the aforementioned panel immediately after a power off discharge quickly.

[0037] Although it explained with reference to the operation gestalt consider that is [this invention] the most practical and desirable as mentioned above, this invention is not limited to these operation gestalt, but is interpreted as the thing containing the various deformation rather contained in the pneuma and domain of a claim, and the equivalent.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] In the LCD containing the gate-on / OFF-state-voltage generator which has a gate-on terminal It has the gate, the source, and a drain, a drain is connected with the aforementioned gate-on terminal, the source is grounded, and it responds to a gate voltage. A turn on or the transistor by which a turn-off is carried out, The diode with which the 1st voltage is impressed to an anode and a cathode is connected with the gate of the aforementioned transistor, The 2nd voltage is impressed to an end child and an other end child contains the capacitor connected with the contact between the cathode of the aforementioned diode, and the gate of the aforementioned transistor. The power-off electric discharge circuit where the turn-off of the transistor is carried out by the potential of the aforementioned contact in the power-on status, and the turn on of the transistor is carried out by the potential of the aforementioned contact in the power-off status.
[Claim 2] The aforementioned transistor is a power-off electric discharge circuit according to claim 1 which is NMOS.
[Claim 3] When the 1st threshold voltage and the threshold voltage of the aforementioned diode are called 2nd threshold voltage for the threshold voltage of the aforementioned transistor, In the power-on status, the 1st aforementioned voltage has a parvus value more from (the 1st threshold voltage + 2nd threshold voltage). It is the power-off electric discharge circuit according to claim 1 or 2 where the 2nd aforementioned voltage has a parvus value more from (the 1st voltage-1st threshold voltage-2nd threshold voltage), and the 1st aforementioned voltage and the 2nd voltage consist of grounding level in the power-off status.
[Claim 4] The liquid crystal panel with which it has many gate lines, the pixel of one line is connected with each aforementioned gate line, and the hold capacitor which is each aforementioned pixel is connected with the gate line of the preceding paragraph, The gate-on / OFF-state-voltage generator which has the gate-on terminal and gate off terminal for generating gate-on / OFF state voltage and outputting the aforementioned voltage, The gate-on / OFF state voltage outputted from the aforementioned gate-on / OFF-state-voltage generator are inputted. The gate drive circuit which chooses the aforementioned gate-on or OFF state voltage to each gate line according to a predetermined control signal, and impresses the voltage by which selection was carried out [aforementioned] to each gate line, It has the gate, the source, and a drain, a drain is connected with the aforementioned gate-on terminal, the source is grounded, and it responds to a gate voltage. A turn on or the transistor by which a turn-off is carried out, The diode with which the 1st voltage is impressed to an anode and a cathode is connected with the gate of the aforementioned transistor, The 2nd voltage is impressed to an end child and an other end child contains the capacitor connected with the contact between the cathode of the aforementioned diode, and the gate of the aforementioned transistor. The LCD containing the power-off electric discharge circuit where the turn-off of the transistor is carried out by the potential of the aforementioned contact in the power-on status, and the turn on of the transistor is carried out by the potential of the aforementioned contact in the power-off status.
[Claim 5] The transistor of the aforementioned power-off electric discharge circuit is a LCD according to claim 4 which is NMOS.
[Claim 6] If the 1st threshold voltage and threshold voltage of the aforementioned diode are made into the 2nd threshold voltage, the threshold voltage of the aforementioned transistor In the

into the 2nd threshold voltage, the threshold voltage of the aforementioned transistor In the power-on status, the 1st aforementioned voltage has a parvus value more from (the 1st threshold voltage + 2nd threshold voltage). It is the LCD according to claim 4 or 5 from which it has a parvus value more from the 2nd aforementioned voltage (the 1st voltage-1st threshold voltage-2nd threshold voltage), and the 1st aforementioned voltage and the 2nd voltage serve as grounding level in the power-off status.

[Claim 7] In the LCD containing the gate-on / OFF-state-voltage generator which has a gate-on terminal It has the gate, the source, and a drain, a drain is connected with the aforementioned gate-on terminal, the source is grounded, and it responds to a gate voltage. A turn on or the transistor by which a turn-off is carried out, The inverter which it has an input edge, an outgoing end, a power edge, and a grounding edge, supply voltage is impressed to an input edge, and the aforementioned outgoing end is connected with the gate of the aforementioned transistor, and provides an outgoing end with the power of a power edge or a grounding edge according to the status of the aforementioned supply voltage, The 1st resistance connected between the input edge of the aforementioned inverter and a power edge and the 1st capacitor connected between the power edge of the aforementioned inverter and a grounding edge are included. In the power-on status, the aforementioned supply voltage is high-level, and the aforementioned supply voltage is a low in the power-off status, and since the moment aforementioned supply voltage of a power off is transmitted to the account power edge of back to front delayed during predetermined time The voltage of the power edge of the account inverter of direct back to front of a power off is a power-off electric discharge circuit which it is provided [circuit] for an outgoing end and carries out the turn on of the aforementioned transistor.

[Claim 8] The aforementioned time delay is a power-off electric discharge circuit according to claim 7 determined according to the time constant by the 1st aforementioned resistance and the 1st capacitor.

[Claim 9] pMOS transistor by which a drain is connected with the aforementioned outgoing end by, as for the aforementioned inverter, connecting the source with the aforementioned power edge, and connecting the gate with the aforementioned input edge, and the source are the power-off electric discharge circuit according to claim 7 which it connects with the aforementioned grounding edge, and the gate is connected with the aforementioned input edge, and consists of an NMOS transistor by which a drain is connected with the aforementioned outgoing end.

[Claim 10] The power-off electric discharge circuit according to claim 7 which contains further, the 2nd resistance connected between the outgoing end of the aforementioned inverter, and the gate of the aforementioned transistor, and the 2nd capacitor which an end is grounded, and the other end is connected with the contact between the 2nd aforementioned resistance and the gate of the aforementioned transistor, and is charged with the voltage of the outgoing end of the aforementioned inverter.

[Claim 11] The turn-on time of the aforementioned transistor just behind a power off is a power-off electric discharge circuit according to claim 10 determined with the time constant by the 2nd aforementioned resistance and the 2nd capacitor.

[Claim 12] The liquid crystal panel with which it has many gate lines, the pixel of one line is connected with each aforementioned gate line, and the hold capacitor which is each aforementioned pixel is connected with the gate line of the preceding paragraph, The gate-on / OFF-state-voltage generator which has the gate-on terminal and gate off terminal for generating gate-on / OFF state voltage and outputting the aforementioned voltage, The gate-on / OFF state voltage outputted from the aforementioned gate-on / OFF-state-voltage generator are inputted. The gate drive circuit which chooses the aforementioned gate-on or OFF state voltage to each gate line according to a predetermined control signal, and impresses the voltage by which selection was carried out [aforementioned] to each gate line, It has the gate, the source, and a drain, a drain is connected with the aforementioned gate-on terminal, the source is grounded, and it responds to a gate voltage. A turn on or the transistor by which a turn-off is carried out, The inverter which it has an input edge, an outgoing end, a power edge, and a grounding edge, supply voltage is impressed to an input edge, and the aforementioned outgoing end is connected with the gate of the

aforementioned transistor, and provides an outgoing end with the power of a power edge or a grounding edge according to the status of the aforementioned supply voltage, The 1st resistance connected between the input edge of the aforementioned inverter and a power edge and the 1st capacitor connected between the power edge of the aforementioned inverter and a grounding edge are included. In the power-on status, the aforementioned supply voltage is high-level, and the aforementioned supply voltage is a low in the power-off status, and since the moment aforementioned supply voltage of a power off is transmitted to the account power edge of back to front delayed during predetermined time The voltage of the power edge of the aforementioned inverter just behind a power off is a LCD containing the power-off electric discharge circuit which it is provided [circuit] for an outgoing end and carries out the turn on of the aforementioned transistor.

[Claim 13] The aforementioned time delay is a LCD according to claim 12 determined according to the time constant by the 1st aforementioned resistance and the 1st capacitor.

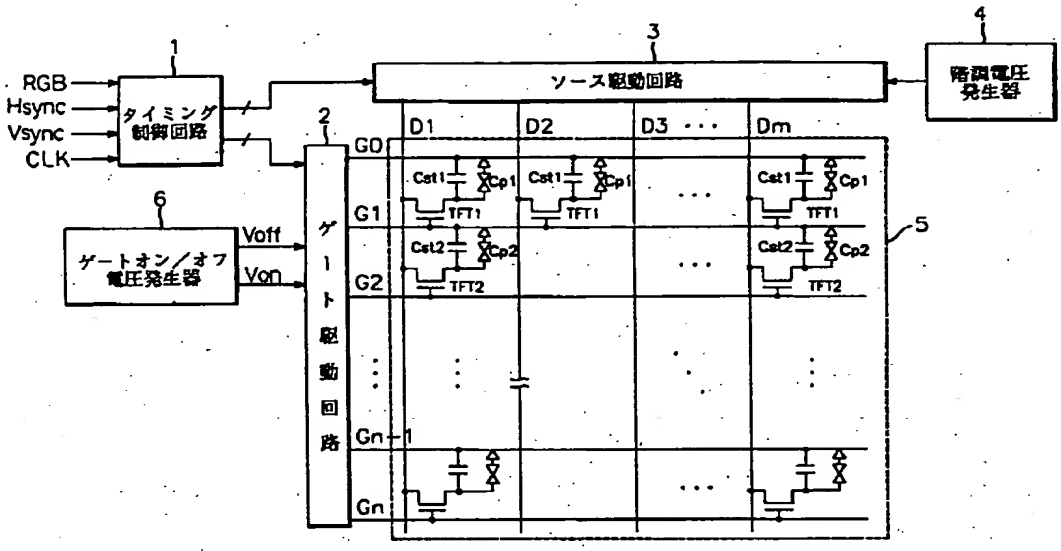
[Claim 14] pMOS transistor by which a drain is connected with the aforementioned outgoing end by, as for the inverter of the aforementioned power-off electric discharge circuit, connecting the source with the aforementioned power edge, and connecting the gate with the aforementioned input edge, and the source are the LCD according to claim 12 which it connects with the aforementioned grounding edge, and the gate is connected with the aforementioned input edge, and consists of an NMOS transistor by which a drain is connected with the aforementioned outgoing end.

[Claim 15] The aforementioned power-off electric discharge circuit is a LCD according to claim 12 which contains further the 2nd resistance connected between the outgoing end of the aforementioned inverter, and the gate of the aforementioned transistor, and the 2nd capacitor which an end is grounded, and the other end is connected with the contact between the 2nd aforementioned resistance and the gate of the aforementioned transistor, and is charged with the voltage of the outgoing end of the aforementioned inverter.

[Claim 16] The turn-on time of the account transistor of direct back to front of a power off is a LCD according to claim 15 determined with the time constant by the 2nd aforementioned resistance and the 2nd capacitor.

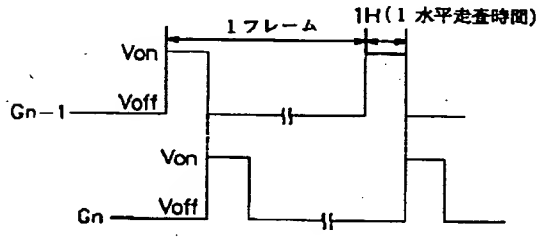
[Translation done.]

Drawing selection Drawing 1



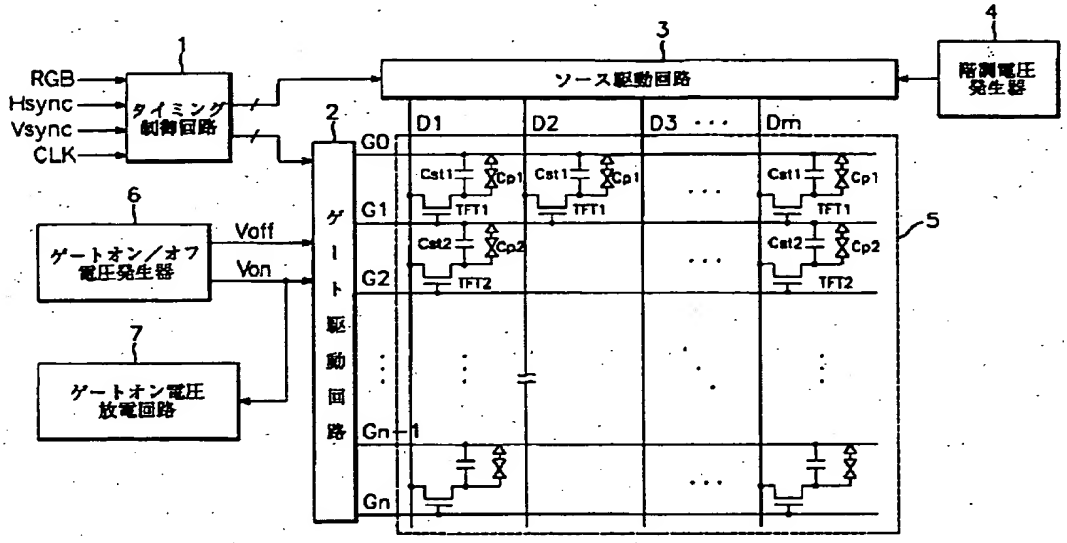
[Translation done.]

Drawing selection Drawing 2



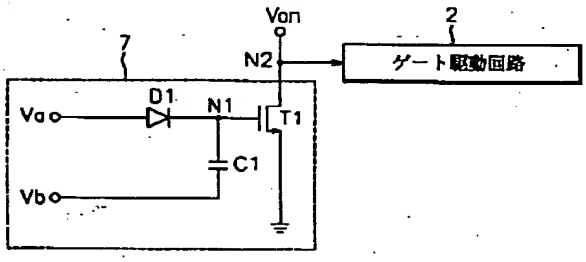
[Translation done.]

Drawing selection Drawing 3



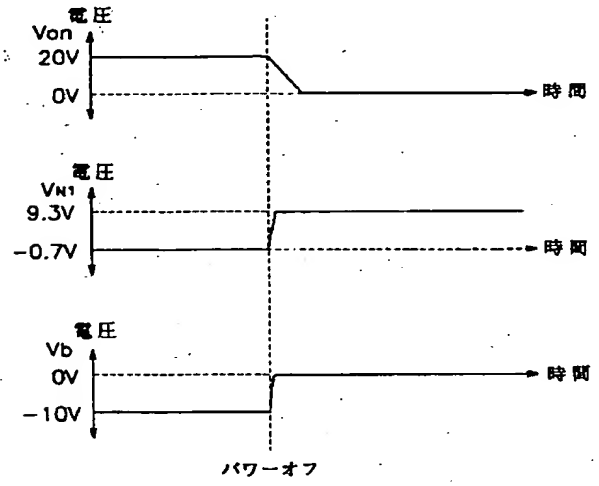
[Translation done.]

Drawing selection Drawing 4



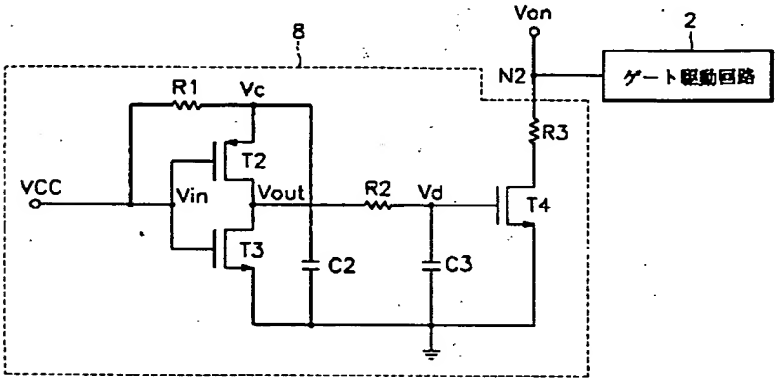
[Translation done.]

Drawing selection Drawing 5



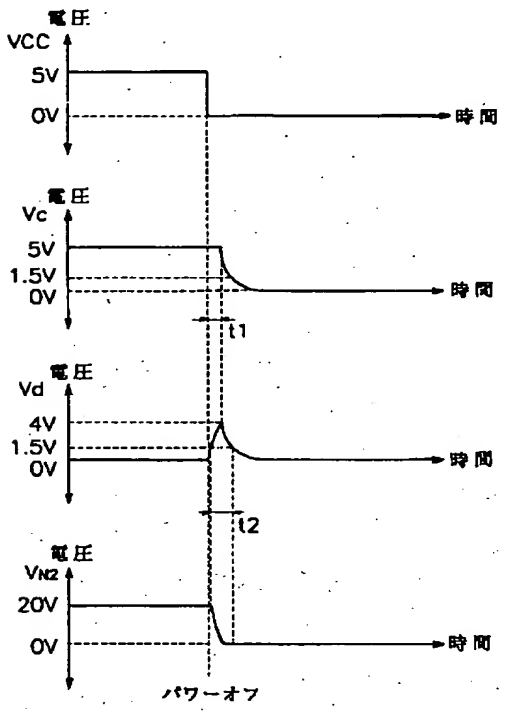
[Translation done.]

Drawing selection Drawing 6



[Translation done.]

Drawing selection Drawing 7



[Translation done.]